TITLE: METHOD AND APPARATUS FOR ADDRESS FIFO FOR HIGH-BANDWIDTH COMMAND/ADDRESS BUSSES IN DIGITAL STORAGE SYSTEM
Inventor: Brian Johnson
Docket No.: 2269-4196.1US

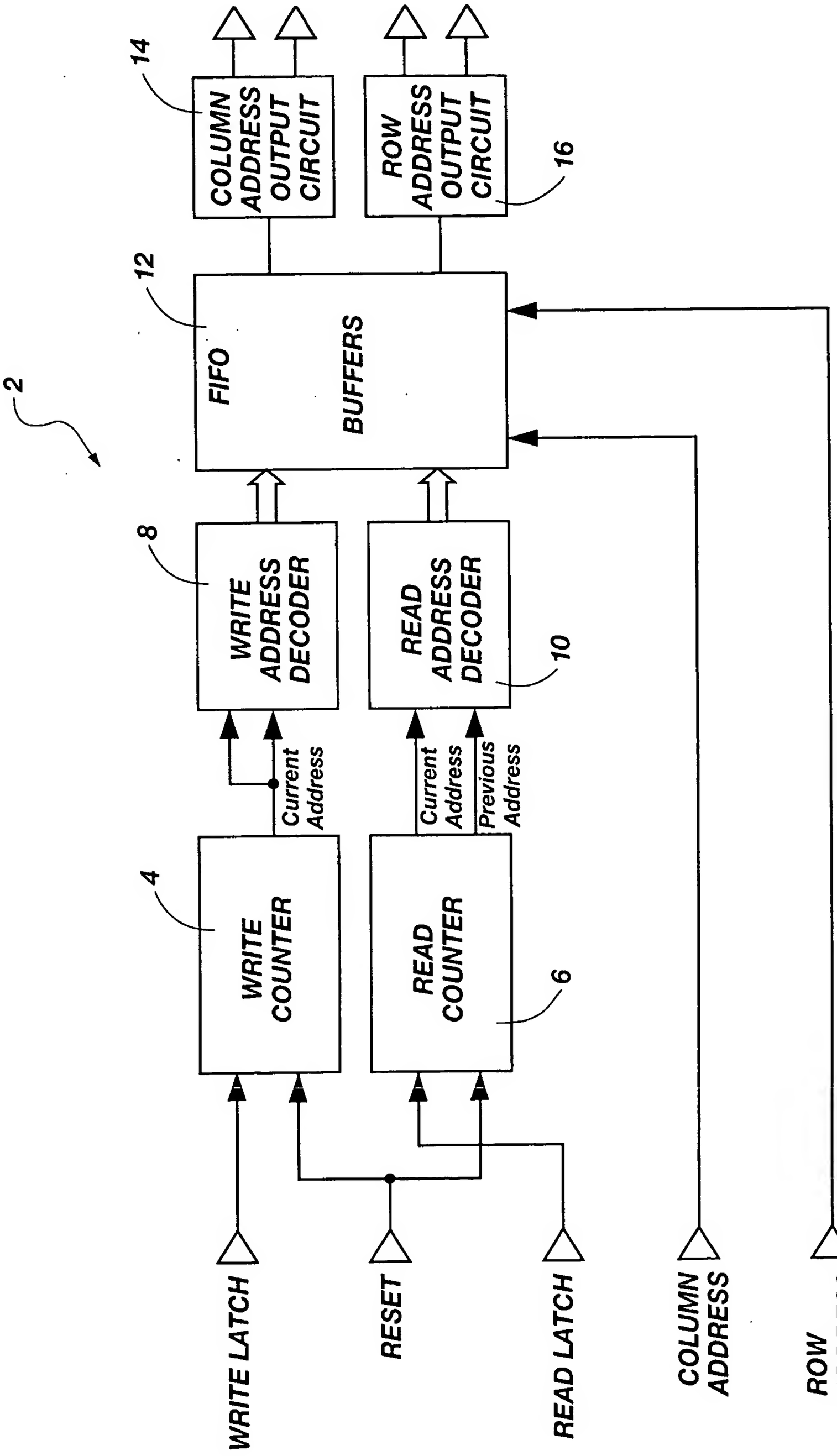

Fig. 1

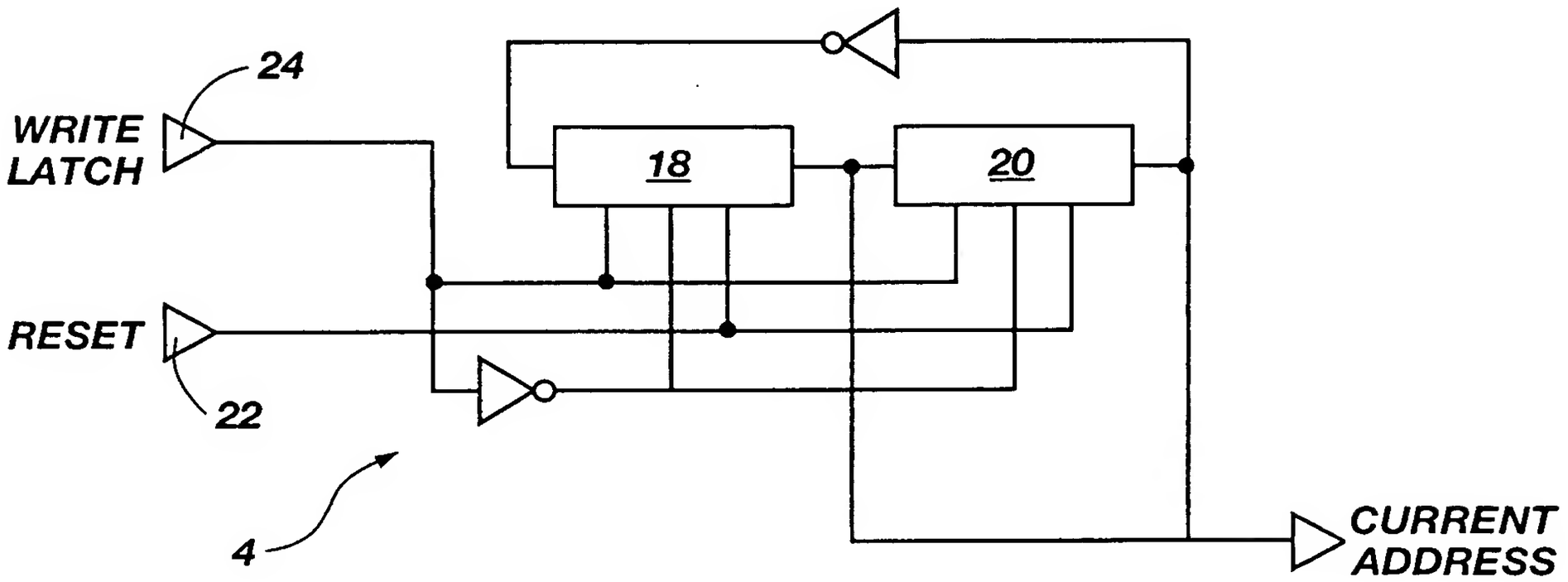

Fig. 2

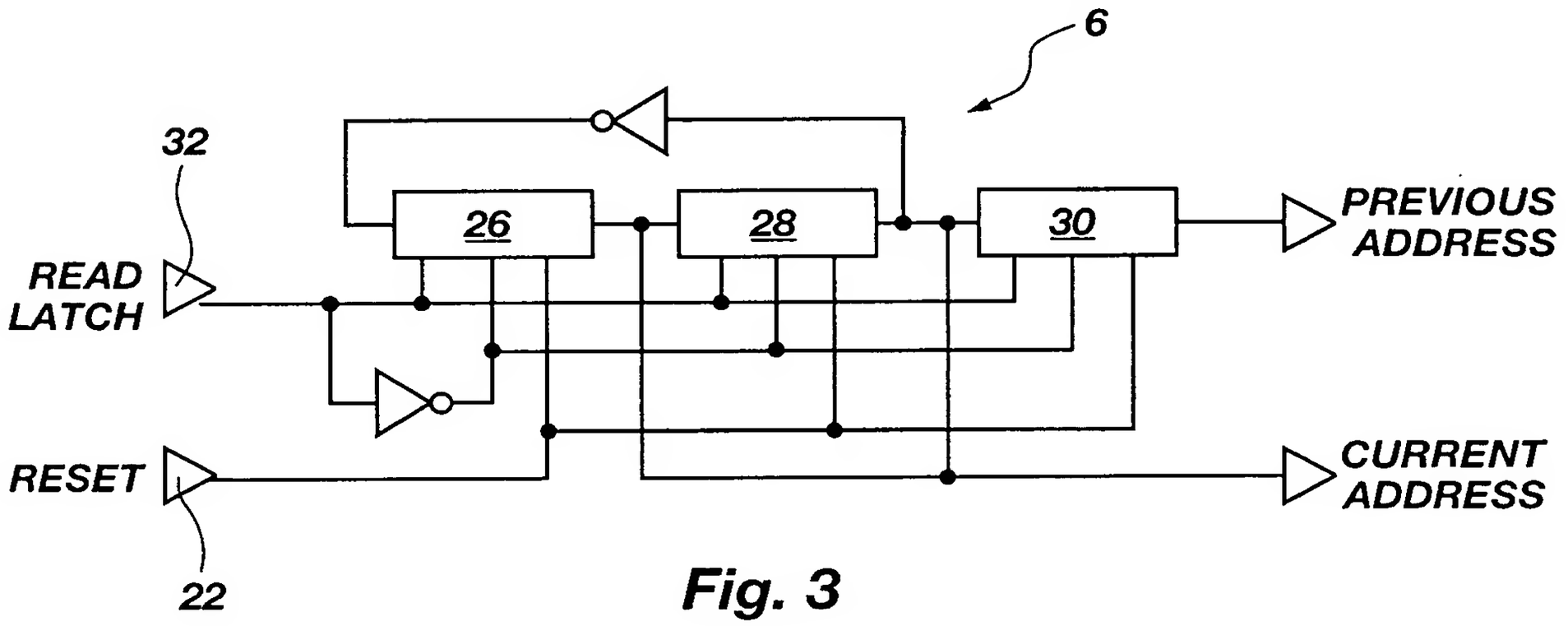

Fig. 3

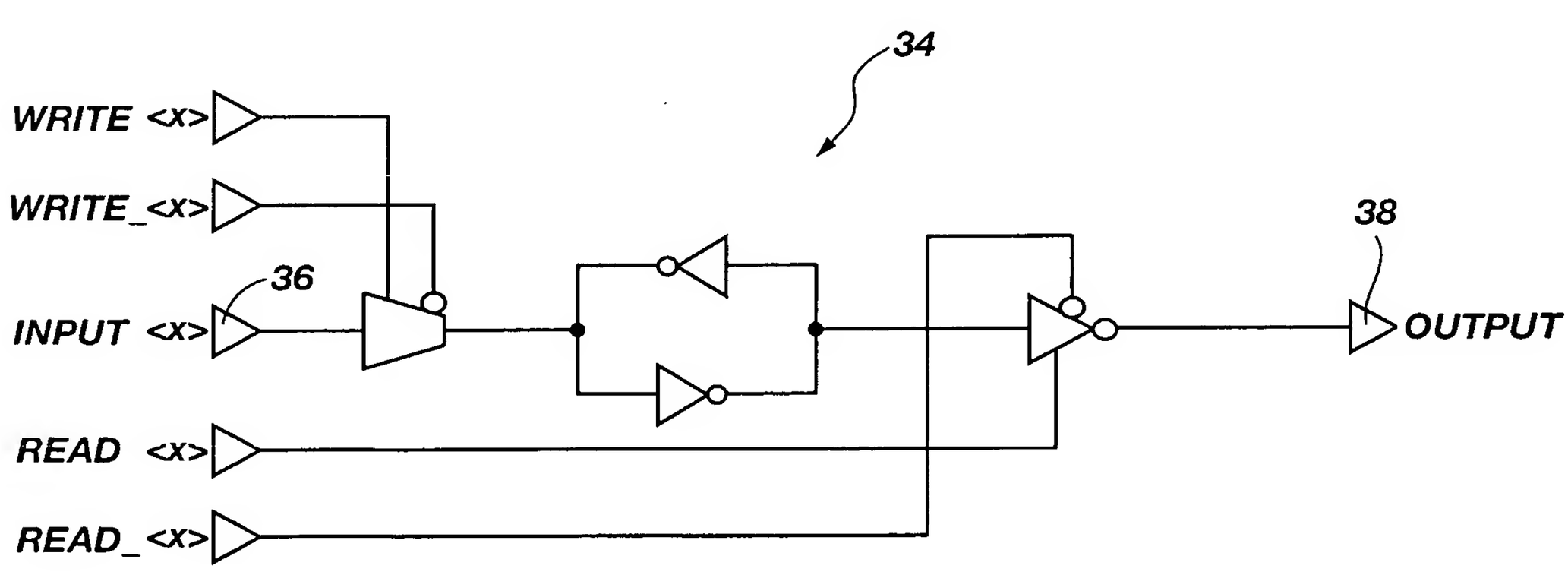

Fig. 4

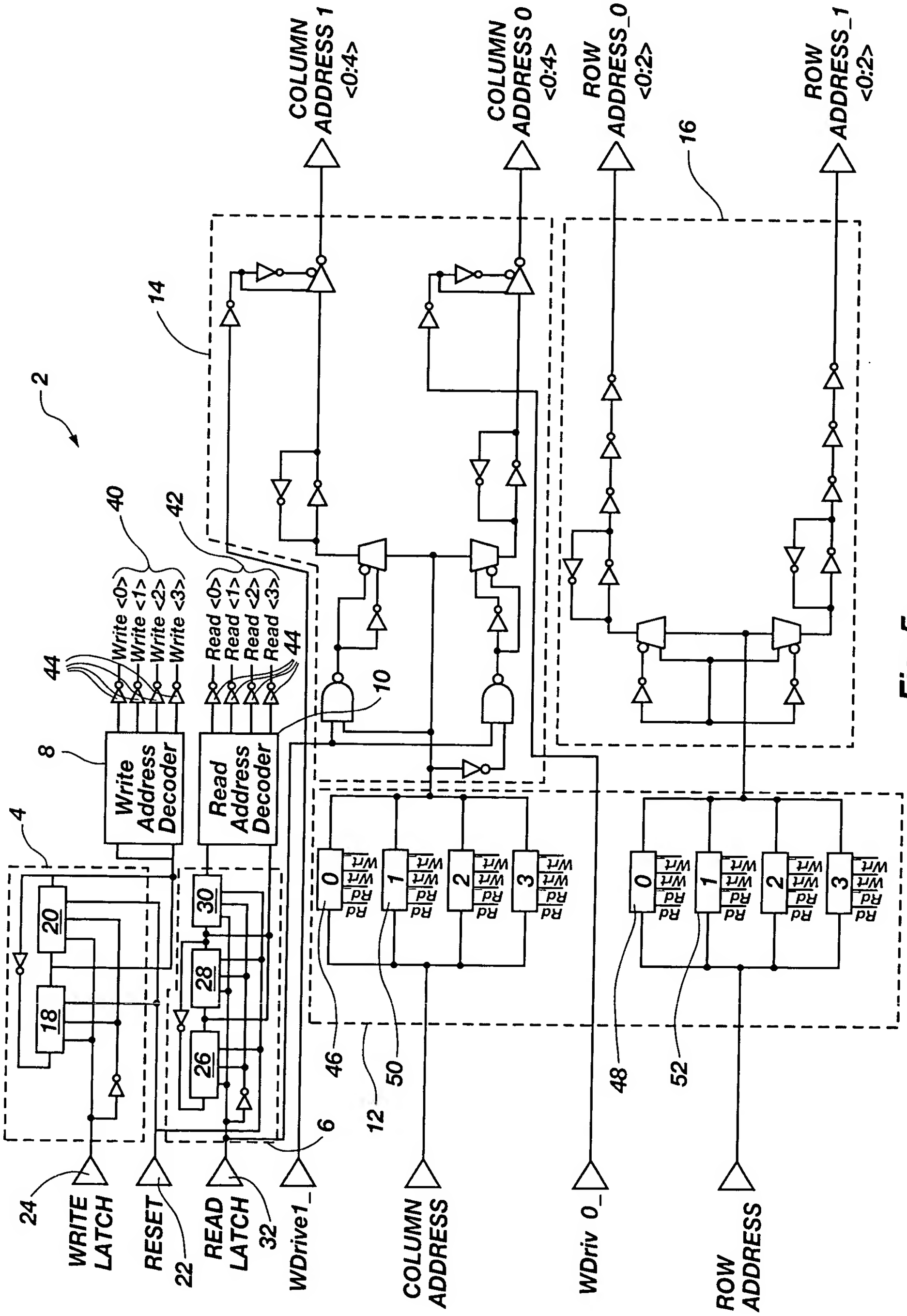
COLUMN ADDRESS 1 <0:4>
COLUMN ADDRESS 0 <0:4>
ROW ADDRESS_0 <0:2>
ROW ADDRESS_1 <0:2>
16
14
2
40
42
Write <0>
Write <1>
Write <2>
Write <3>
Read <0>
Read <1>
Read <2>
Read <3>
44
44
10
8
Write Address Decoder
Read Address Decoder
4
20
18
30
28
26
Wt
Rd
0
1
2
3
46
50
12
48
52
6
24
32
22
WRITE LATCH
RESET
READ LATCH
WDrive1_
COLUMN ADDRESS
WDriv 0_
ROW ADDRESS

Fig. 5

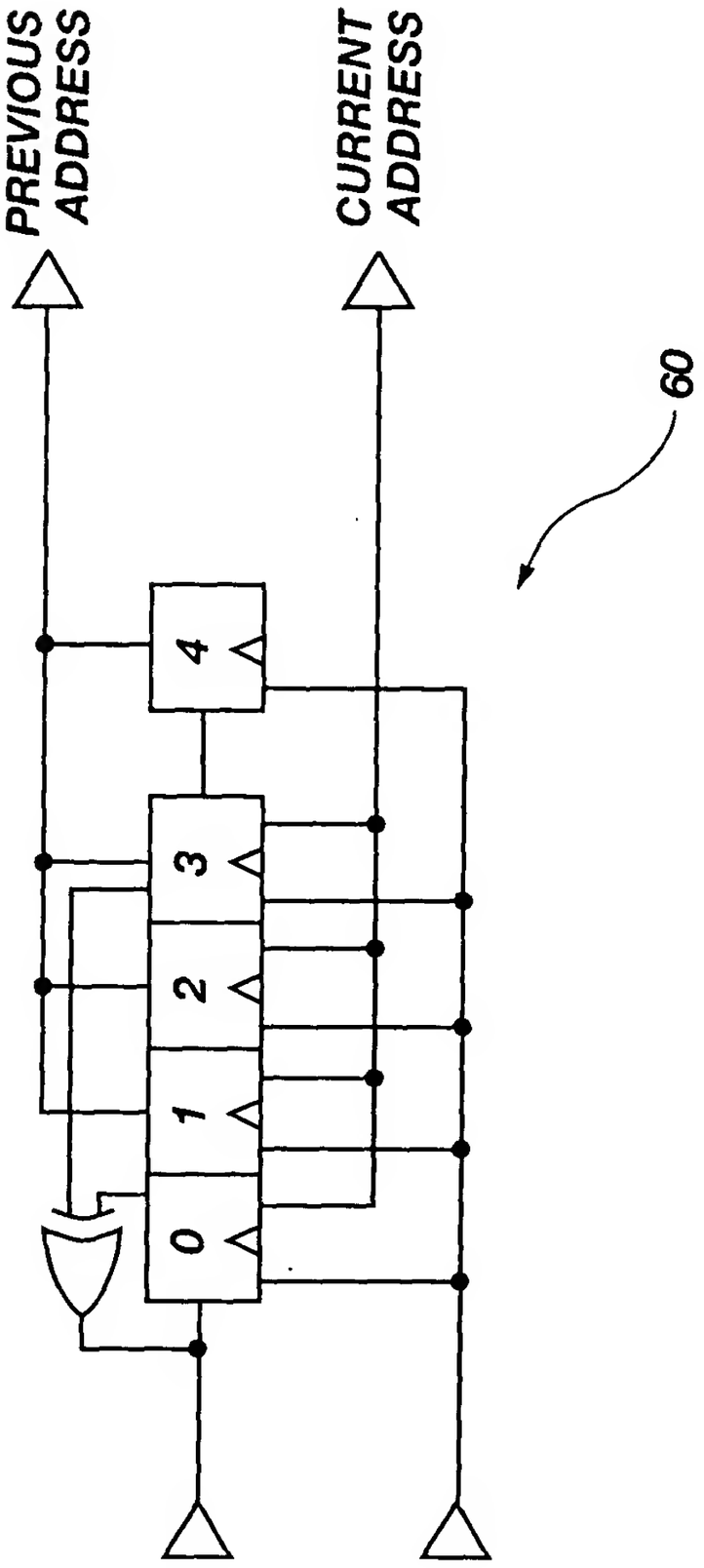
PREVIOUS ADDRESS
CURRENT ADDRESS
READ LATCH
RESET
60
4
3
2
1
0

Fig. 6

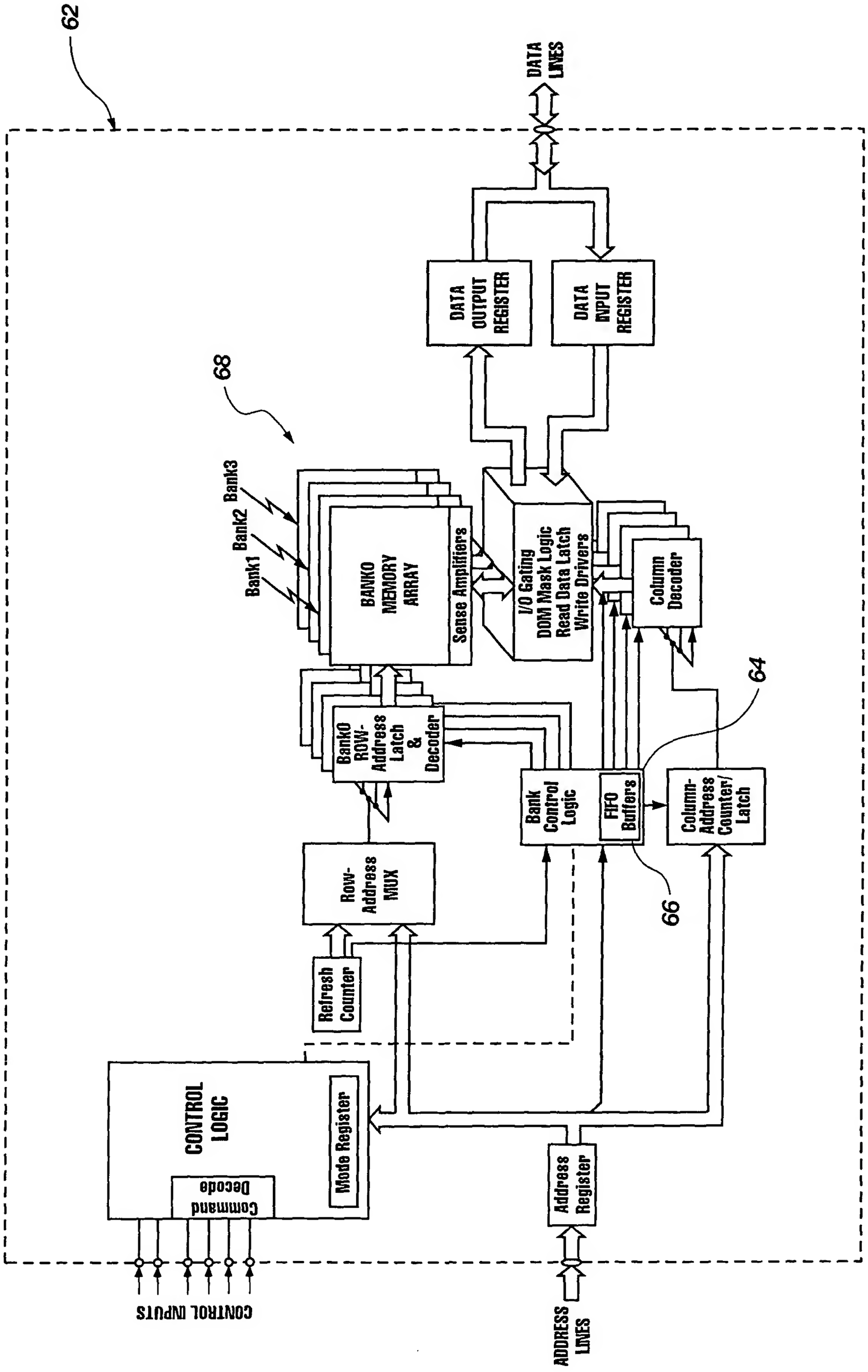
62
DATA LINES
DATA OUTPUT REGISTER
DATA INPUT REGISTER
68
Bank3
Bank2
Bank1
BANK0 MEMORY ARRAY
Sense Amplifiers
I/O Gating DQM Mask Logic Read Data Latch Write Drivers
Column Decoder
Bank0 ROW-Address Latch & Decoder
64
Bank Control Logic
FIFO Buffers
Column-Address Counter/ Latch
Row-Address MUX
66
Refresh Counter
CONTROL LOGIC
Command Decode
Mode Register
Address Register
CONTROL INPUTS
ADDRESS LINES

Fig. 7

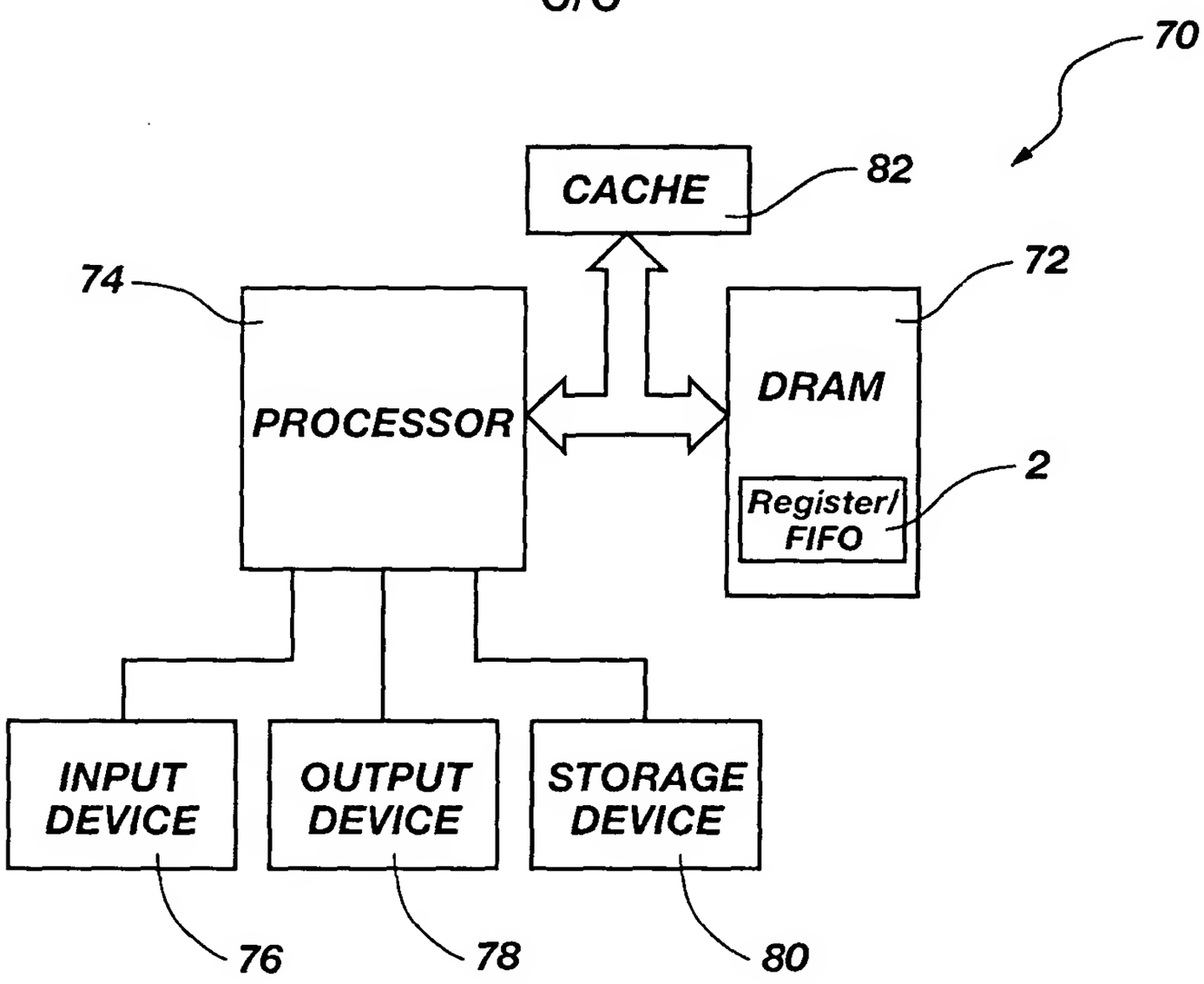
70
CACHE
82
74
72
PROCESSOR
DRAM
Register/
FIFO
2
INPUT
DEVICE
OUTPUT
DEVICE
STORAGE
DEVICE
76
78
80

Fig. 8

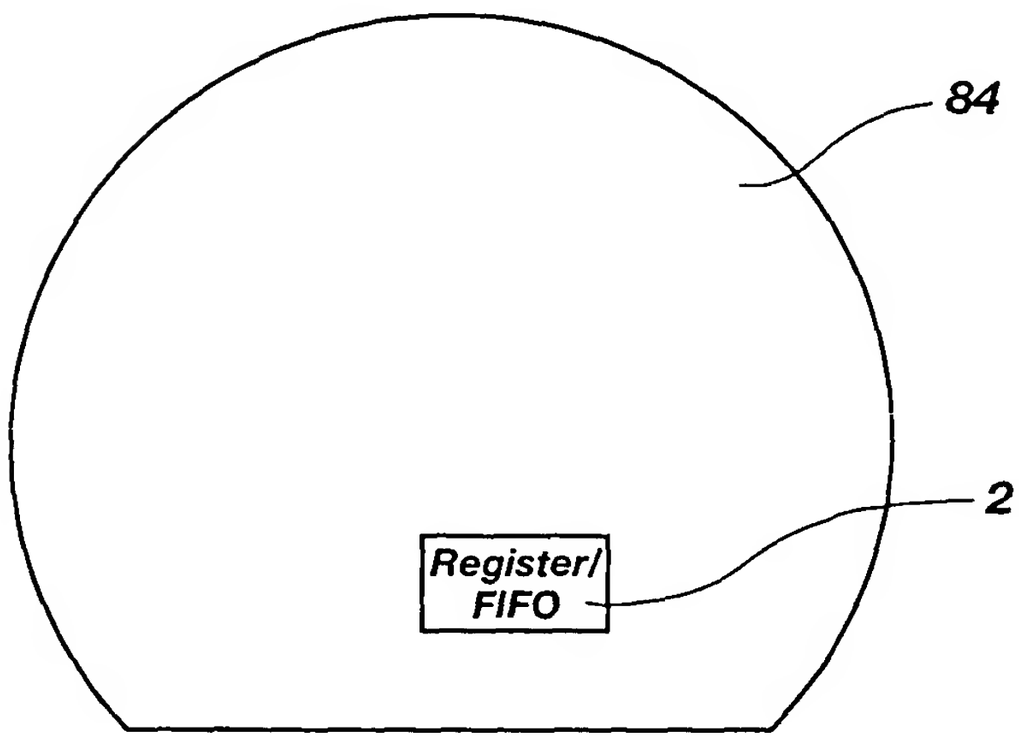
84
Register/
FIFO
2

Fig. 9